

FIG. 1 is a block diagram of a digital circuit 1. The circuit includes a first D-type flip-flop 6, a second D-type flip-flop 7, a third D-type flip-flop 5, and a fourth D-type flip-flop 9. A first multiplexer 3 has two data inputs, 0 and 1, and an enable input. A second multiplexer 8 has two data inputs, 0 and 1, and a select input. The circuit is clocked by two signals, CLOCK A and CLOCK B. The output of the first multiplexer 3 is DATA IN 2. The output of the second multiplexer 8 is DATA OUT. The circuit also includes an inverter 4 and a delay element 5.

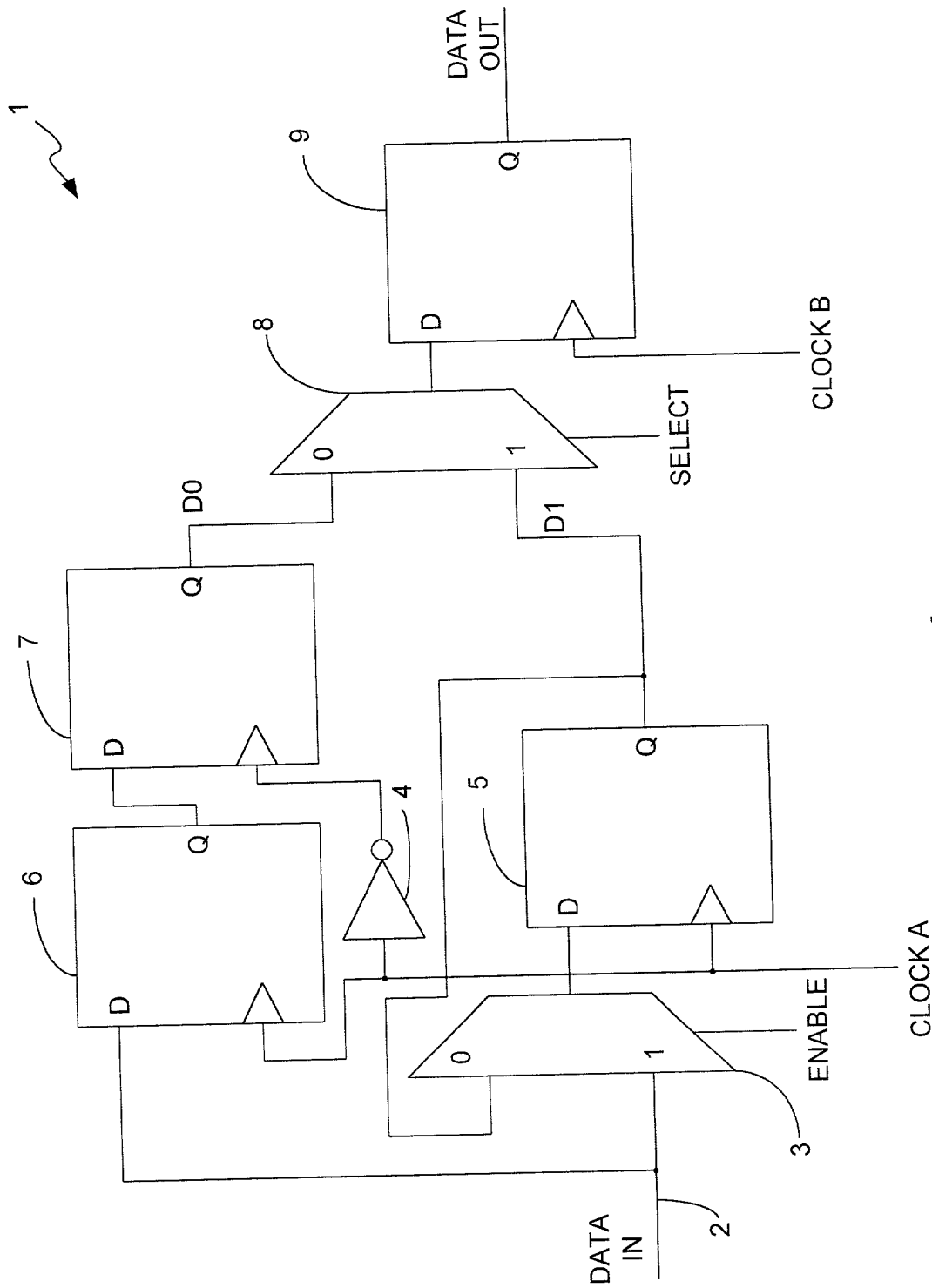
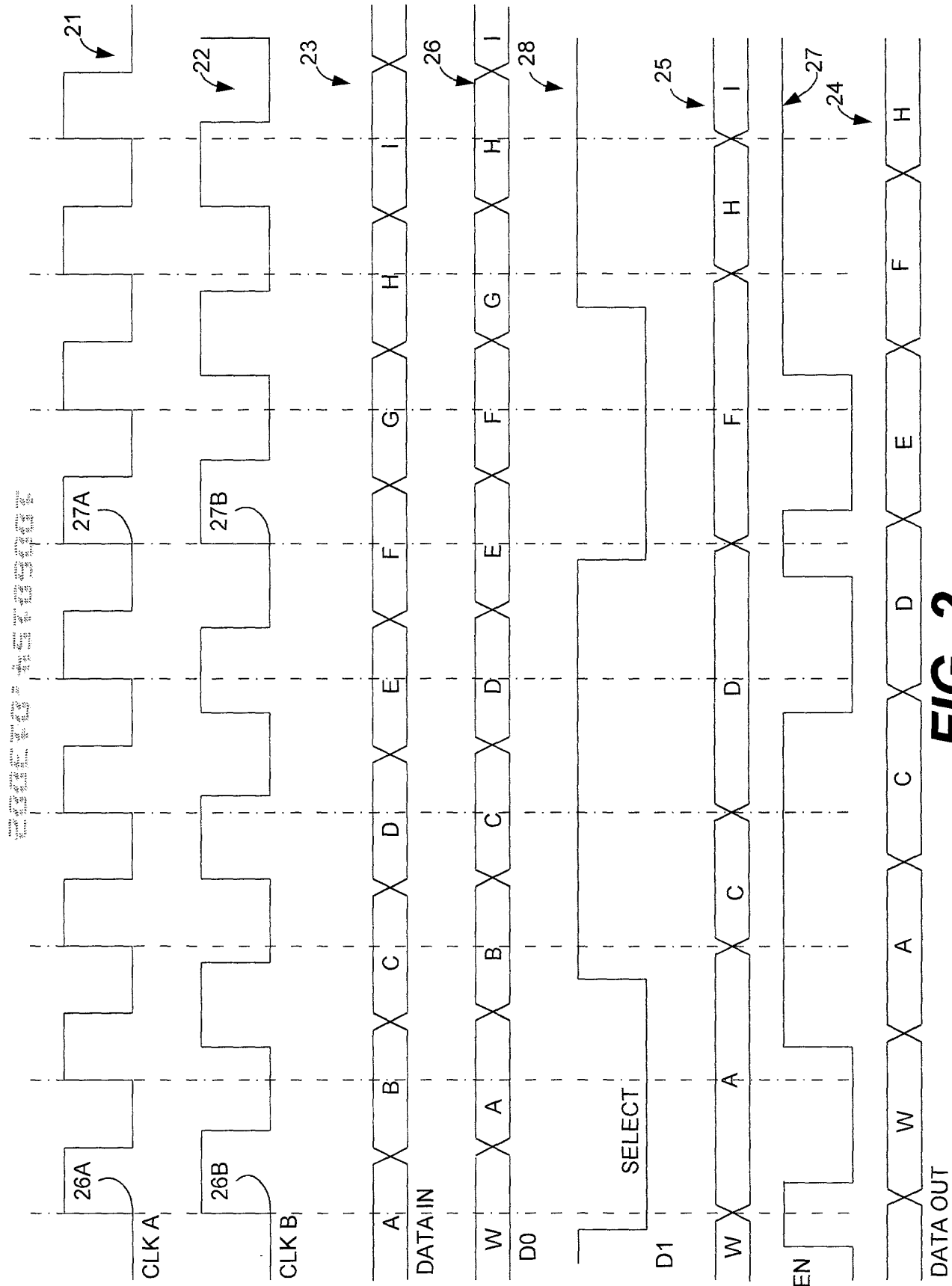
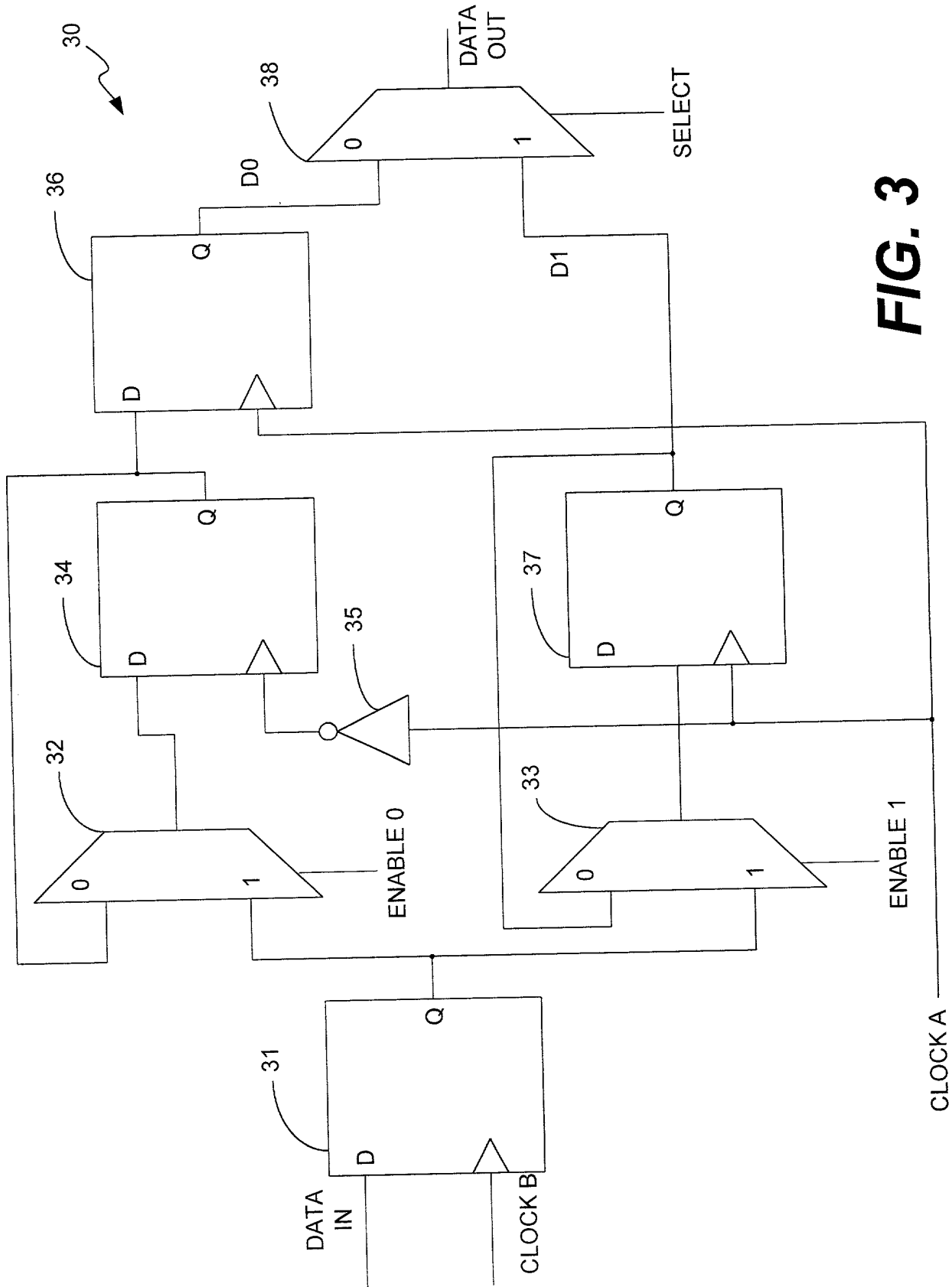


FIG. 1

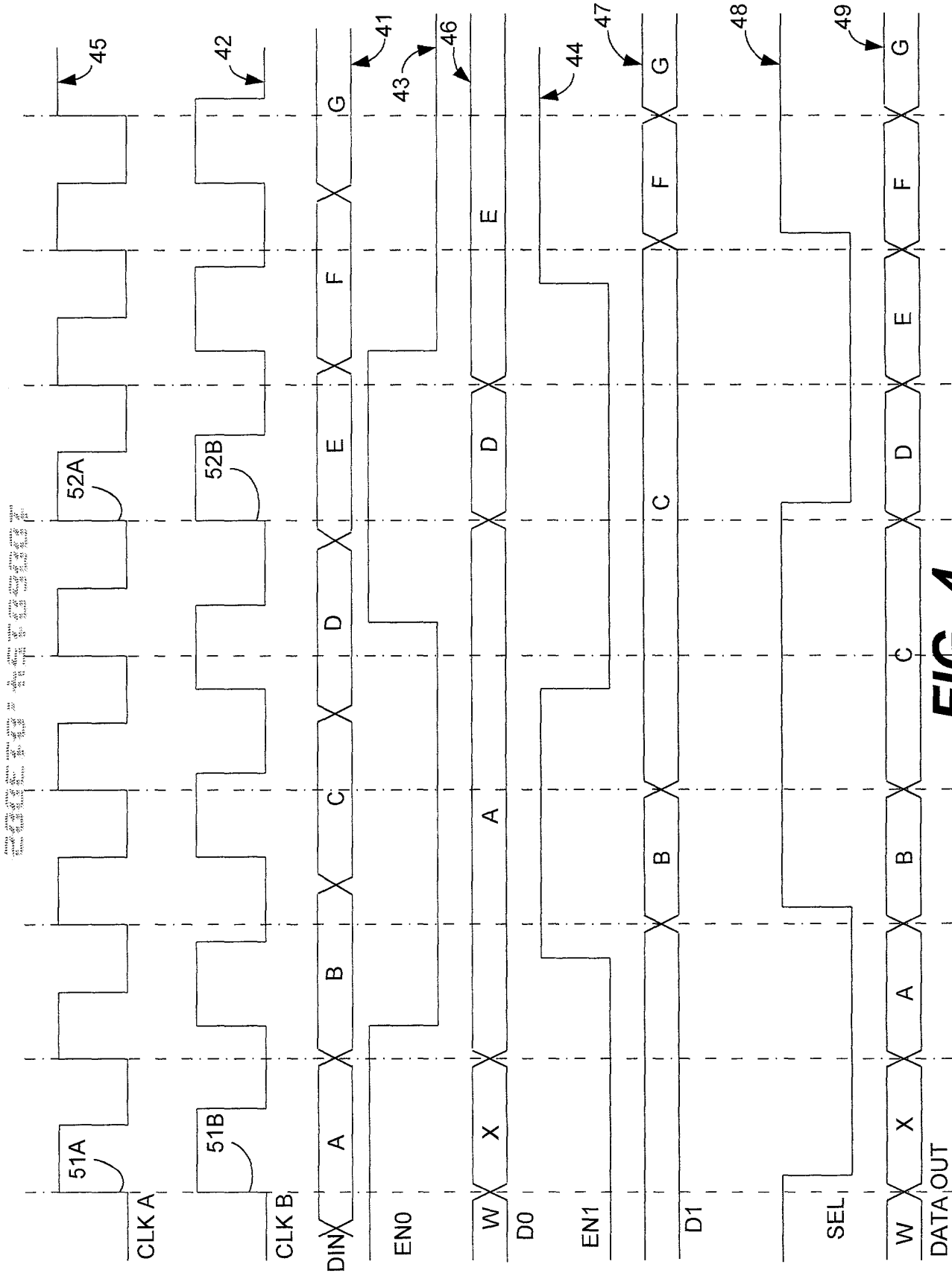


**FIG. 2**

FIG. 3 is a block diagram of a digital circuit 30. The circuit 30 includes a first D-type flip-flop 31, a second D-type flip-flop 32, a third D-type flip-flop 33, a fourth D-type flip-flop 34, a fifth D-type flip-flop 35, a first 2-to-1 multiplexer 36, a second 2-to-1 multiplexer 37, and a third 2-to-1 multiplexer 38. The circuit 30 is configured to perform a specific function, such as a data path or a control logic.



**FIG. 3**



**FIG. 4**